Roll No. .

Total Pages : 05

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B.Tech. EXAMINATION, 2022

Semester III (CBCS)

COMPUTER ARCHITECTURE AND ORGANIZATION (CSE, IT)

CS-303

Time : 3 Hours *Maximum Marks : 60*

The candidates shall limit their answers precisely within the answer book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt *Five* questions in all, selecting *one* question from each Sections A, B, C and D. Q. No. 9 is compulsory.

Section A

1. (a) What do you mean by flip-flops ? Describe the different types of flip-flops with suitable examples. 5

(b) A digital computer has a common bus system for 16 registers of 32-bits each : 5

(i) How many selection input are there in each multiplexer ?

(ii) What size of multiplexer is needed ?

(iii) How many multiplexer are there in a bus ?

2. (a) What is three-state bus buffer ? Explain the operation of three-state bus buffer and show its use in design of common bus. 5

(b) The two numbers given below are multiplied using the Booth's algorithm :

Multiplicand : 0101 1010 1110 1110

Multiplier : 0111 0111 1011 1101

How many additions/subtractions are required for the multiplication of the above two numbers ? 5

Section B

3. (a) List and explain memory-reference instructions with the help of flow chart. Also give example of each instruction. 6

(b) Explain the basic working principle of the control unit with timing diagram. 4

4. (a) Consider a three word machine instruction :
ADD A[R20], @B
The first operand (destination) "A[R0]" uses indexed addressing mode with R0 as the index register. The second operand (source) "@B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand). What is the number of memory cycles needed during the execution cycle of the instruction ? 7

(b) Write a short note on different Addressing Modes. 3

Section C

5. (a) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes ? How many lines of address bus must be used to access 2048 bytes of memory ? How many of these lines will be common to all chips ? How many lines must be decoded for the chip select ? Specify the size of the decoder. 4

(b) Why does DMA have priority over CPU who requests a memory transfer ? Explain DMA in detail. 6

6. Explain Program Interrupts. Explain clearly, discussing the role of stack, PSW and return from interrupts instruction, how interrupts are implemented on computers ? 10

Section D

7. Explain Flynn's classification of computers in detail with a diagram. Also write the differences between MISD and MIMD. 10

8. (a) Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate : 6

(i) Pipeline cycle time
(ii) Non-pipeline execution time
(iii) Speed up ratio
(iv) Pipeline time for 1000 tasks
(v) Sequential time for 1000 tasks
(vi) Throughput.

(b) Write a short note on various Performance Evaluation benchmarks. Enlist the differences between Wheatstone and Drystone. 4

(Compulsory Question)

9. Short answer type questions :

(i) What are the advantages and disadvantages of microprogramming ? 2

(ii) Define the term LRU and LFU. 2

(iii) Explain in brief the significance of cache memory. 2

(iv) Write down the expressions for speedup factors in a pipelined architecture. 2

(v) Define intra segment and inter segment communication. 2

(vi) What is bus arbitration ? 2

(vii) What is the difference between the restoring and non-restoring method of division ? 2

(viii) What do you mean by address space and memory space in virtual memory ? 2

(ix) What is Sequencer ? Mention its functions. 2

(x) What are write-through and write-back cache write-methods ? 2